REMARKS/ARGUMENTS

In response to the Office Action dated August 6, 2003, claims 4, 6, 20, 22, and 24 are amended, and claims 2 and 23 are canceled without prejudice or waiver. Claims 4, 6, 19-22 and 24 remain in the application. It is not the Applicants' intent to surrender any equivalents because of the amendments or arguments made herein. Reexamination and reconsideration of the application are respectfully requested.

Non-Art-Based Rejections

In paragraphs 3-4 of the Office Action, claim 4 was rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement and that claim 4 contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor had possession of the claimed invention. Specifically, the Office Action refers to the electric charge accumulating portion not being mentioned in the specification or the drawings.

Applicant respectfully traverses the rejection.

> A gate structure in this embodiment is different from that in the preceding embodiment, wherein neither the floating gate 4 nor the inter-layer insulating layer 5 is formed, and an insulating layer 20 under the control gate 6 takes a 3 layered structure consisting of a silicon oxide layer (a tunnel oxide layer) 21, a silicon nitride layer 22 and a silicon oxide layer 23. This functions as an electric charge accumulating portion in which the electrons are trapped by an interface level between the silicon oxide layer 21 and the silicon nitride layer 22 of the stack-structured insulating layer 20.

See original specification, page 12, lines 6-16, and FIG. 3.

Since the charge accumulation portion is disclosed in the specification and the figures, the Applicant respectfully requests that the rejection be withdrawn.

Art-Based Rejections

In paragraph 7 of the Office Action, claims 2, 19, and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lu et al., USPN 6,130,452 in view of Kume et al, (IEDM 87).

In paragraph 8 of the Office Action, claims 4 and 21-23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lu et al., USPN 6,130,452 in view of Kume et al, (IEDM 87), and further in view of Okuda et al., USPN 5,640,345.

In paragraph 9 of the Office Action, claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lu et al., USPN 6,130,452 in view of Kume et al, (IEDM 87), and further in view of Sung et al., USPN 5,631,179.

In paragraph 10 of the Office Action, claim 24 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lu et al., USPN 6,130,452 in view of Kume et al, (IEDM 87), and Okuda et al., USPN 5,640,345, and further in view of Sung et al., USPN 5,631,179.

The Applicant respectfully traverses the rejections, however, in order to expedite prosecution, the Applicants have amended the claims. The Applicants respectfully submit that the claims are patentable in light of the clarifying amendments above and the arguments below.

The Lu Reference

The Lu reference discloses a virtual ground flash cell with asymmetrically placed source and drain. The drain diffusion is formed from an n+ diffusion 118a and an n- diffusion 118b. The drain diffusions 118a-b both overlap the bird's beak encroachment 116a and extend to a thin tunneling region 124a. The source diffusion is an n-type dopant 120. The source diffusion underlaps 124b the bird's beak encroachment 116b. The thick oxide of the encroachment separates the whole of the source diffusion from the floating gate core and, thereby, minimizes the tunneling of electrons to and from the floating gate on the source side of the cell. See Col. 5, lines 32-41.

The Kume Reference

The Kume reference discloses a flash erase EEPROM cell with an asymmetric source and drain structure. The n- profile in the source region has been determined in consideration of both an n+ -n- -p junction breakdown voltage and a capacitive coupling between the source and the floating gate. See Page 560, Col. 2, 2nd full paragraph.

The Okuda Reference

The Okuda reference discloses a semiconductor memory device and fabrication processes. First gate dielectric layer 11 and second gate dielectric layer 15 each have an energy barrier that is so high as to impede the passage of carriers. With regard to first and second carrier capture layers 12 and 14, they have energy levels capable of capturing carriers. See Col. 7, lines 23-27.

The Sung Reference

The Sung reference discloses a method of manufacturing metallic source line, self-aligned contacts for flash memory devices. There are oxidized sidewalls 28 in trench spaces 22' and 22" formed on the sidewalls of the stacks 50 covering the edge surfaces of gate electrodes 12 and 14, and ONO layer 13. The oxidized sidewalls 28 are formed with a thickness between about 100 Angstroms and about 200 Angstroms. On the sidewalls 28 and on the sidewall edges of dielectric layer 16 and dielectric layer 18 are formed silicon nitride spacers 29' with a thickness between about 1500 Angstroms and about 2000 Angstroms. See Col. 3, line 66-Col. 4, line 7.

The Claims are Patentable over the Cited Reference

The claims of the present invention describe a non-volatile semiconductor memory. A device in accordance with the present invention comprises a semiconductor substrate, a source region provided in said semiconductor substrate, a drain region provided in said semiconductor substrate, said source and drain regions being spaced away from each other, a floating gate provided above a channel region between said source and drain regions, and a control gate provided above said channel region, wherein a writing operation is executed in such a way that hot electrons are generated in the vicinity of said drain region and injected into said floating gate, and an erasing operation is performed by releasing the electrons held by said floating gate into said channel region, wherein an overlap of said drain region with said floating gate is larger than an overlap of said source region with said floating gate, wherein said floating gate is provided between said channel region and said control gate through respective insulating layers, and wherein a

junction depth of said source region is larger than a junction depth of said drain region.

The cited references do not teach nor suggest all of the limitations of the claims of the present invention. Specifically, the cited references do not teach nor suggest the limitations of a writing operation executed in such a way that hot electrons are generated in the vicinity of said drain region wherein an overlap of said drain region with said floating gate is larger than an overlap of said source region with said floating gate as recited in the claims of the present invention.

The main feature of the present invention is that an overlap of a gate and a drain region of a memory cell is larger than an overlap of the gate and a source region, but junction depth of the source region is deeper than that in the drain region.

The memory cell having such structure requires the following memory operation: in writing, hot electrons should be injected into the floating gate from the drain side and in erasing, electrons are not drawn at only source side but drawn at the whole surface of the channel. This results in no necessity of the overlap of the gate and source region.

According to Lu et al., the overlap of the gate and the drain diffusion region is longer than that of the gate and the source diffusion region. However, the longer overlap of the drain side disclosed in Lu is intended to draw electrons to the drain side. Therefore, there is no teaching in Lu that the longer overlap is provided at the diffusion region where hot electrons are injected at the time of writing as recited in the claims of the present invention.

Further, the feature that an overlap of a gate and a drain region of a memory cell is larger than an overlap of the gate and a source region, but the junction depth

of the source region is deeper than the junction depth in the drain region is not disclosed in Lu.

The ancillary Kume reference does not remedy the deficiencies of the Lu reference. Although Kume shows a deeper source diffusion region, which was made deeper in order to apply a higher erase voltage, there is no necessity in the present invention to make the source diffusion region deep in order to apply high erase voltages to the source, since electrons are not drawn to the source diffusion region. Furthermore, according to the present invention, the overlap of the gate and drain diffusion region can be made longer since there is no necessity to elongate the overlap of the gate and the source diffusion region source since electrons are not drawn to the source diffusion region. The purpose of the present invention to make the source junction deep is reduction of source resistance.

Furthermore, Kume's larger source junction depth is used to improve programming efficiency by using the shielding p-pocket layer, which improves injection efficiency.

As such, neither Lu nor Kume teach nor suggest at least the limitation of a writing operation executed in such a way that hot electrons are generated in the vicinity of said drain region wherein an overlap of said drain region with said floating gate is larger than an overlap of said source region with said floating gate as recited in the claims of the present invention.

Further, the ancillary Okuda and Sung references do not remedy the deficiencies of the Lu and Kume references, namely, the Okuda and Sung references do not teach nor suggest at least the limitation of a writing operation executed in such a way that hot electrons are generated in the vicinity of said drain region wherein an overlap of said drain region with said floating gate is larger than an

overlap of said source region with said floating gate as recited in the claims of the present invention.

The Applicant further suggests that it is not possible to combine at least Sung with the remaining references, because although Sung discloses side walls having two layers, the end portion of the upper layer 29 locates the end portion of the lower layer 28, which means such double layer structure of the side wall cannot be used to implant impurity ions to obtain the source and drain regions shown in Figs. 6D or 7D. In other words, the double layer structure of Sung cannot be used to obtain two stage self-aligned ion implantation.

Since the references do not teach nor suggest the limitations of the independent claims 19 and 21, namely, that the cited references do not teach nor suggest at least the limitation of a writing operation executed in such a way that hot electrons are generated in the vicinity of said drain region wherein an overlap of said drain region with said floating gate is larger than an overlap of said source region with said floating gate as recited in the claims of the present invention, the Applicant respectfully submits that claims 19 and 21 are patentable over the cited references.

Claims 4, 6, 20, 22, and 24 are also patentable over the cited references, not only because they contain all of the limitations of the independent claims, but because claims 4, 6, 20, 22, and 24 also describe additional novel elements and features that are not described in the prior art.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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